Switching Theory & Logic Design

By Mr. A P Godse, Mrs D A Godse

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UNIT I (Chapter-1) Review of Number Systems : Representation of numbers of different radix, Conversion of numbers from one radix to another radix, r-1's complement and r's complement of unsigned numbers subtraction, Problem solving. Signed binary numbers, Different forms, Problem solving for subtraction. 4-bit codes : BCD, EXCESS-3, Alphanumeric codes, 9's complement, 2421, etc. UNIT II (Chapter-2) Logic Operation, Error Detection and Correction Codes : Basic logic operations NOT, OR, AND, Boolean theorems, Complement and dual of logical expressions, NAND and NOR Gates, EX-OR, EX-NOR Gates, Standard SOP and POS, Minimization of logic functions using theorems, Generation of self dual functions. Gray code, Error detection and error correction codes, Parity checking even parity, Odd parity, Hamming code, Multi-leveled AND-NOR realizations. Two level NAND-NAND and NOR-NOR realizations. Degenerative forms and multi-level realizations. UNIT III (Chapter-3) Minimization of Switching Functions : Minimization of switching functions using K-Map up to 6-variables, Tabular minimization, Minimal SOP and POS realization. Problem solving using K-map such as code converters binary multiplier etc. UNIT IV (Chapter-4) Combinational Logic Circuits-I : Design of half adder, Full adder, Half subtractor, Full subtractor, Applications of full adders, 4-bit binary adder, 4-bit binary subtractor, Adder-subtractor circuit, BCD adder circuit Excess-3 adder circuit, Look-a-head adder circuit. UNIT V (Chapter-5) Combinational Logic Circuits-II : Design of decoder, Demultiplexer, Higher order demultiplexing, Encoder, Multiplexer, Higher order multiplexer, Realization of Boolean functions using decoders and multiplexers, Priority encoder, Different code converter using full adders. UNIT VI (Chapter-6) Combinational Logic Circuits-III : PROM, PLA, PAL, Realization of switching functions using PROM, PLA and PAL; Comparison of PROM, PLA, and PAL, Programming tables of PROM, PLA and PAL. UNIT VII (Chapter-7) Sequential Circuits - I : Classification of sequential circuits (synchronous and asynchronous): basic flip-flops, Truth tables and excitation tables (NAND RS latch, NOR RS latch, RS flip-flop. JK flip-flop, T flip-flop, D flip-flop with reset and clear terminals).Conversion of flip-flop to flip-flop. Design of ripple counters, Design of synchronous counters, Johnson counters, Ring counters. Design of registers, Buffer register, Control buffer register, Shift register, Bi-directional shift register, Universal shift register. UNIT VIII (Chapter-8) Sequential Circuits-II : Finite state machine, Capabilities and limitations, Analysis of clocked sequential circuits, Design procedures,

Reduction of state tables and state assignment. Realization of circuits using various flip-flops. Mealy to Moore conversion and vice-versa.

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